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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,365	07/23/2003	Richard W. Adkisson	200300031-2	8221

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EXAMINER	
DSOUZA, JOSEPH FRANCIS A	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
01/02/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/625,365	ADKISSON ET AL.	
	Examiner	Art Unit	
	Adolf DSouza	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 7, 9 - 23* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Specification

1. The incorporation of essential material in the specification by reference to an unpublished U.S. application, foreign application or patent, or to a publication is improper. Applicant is required to amend the disclosure to include the material incorporated by reference, if the material is relied upon to overcome any objection, rejection, or other requirement imposed by the Office. The amendment must be accompanied by a statement executed by the applicant, or a practitioner representing the applicant, stating that the material being inserted is the material previously incorporated by reference and that the amendment contains no new matter. 37 CFR 1.57(f).

In the Specification (page 1, paragraph 2), the application number and filing date of the co-pending application is missing.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 5, 9 - 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Garcia et al. (US 6,084,934)** in view of **Audityan et al. (US 6,317,806).**

Regarding claim 1, Garcia discloses a system for effectuating the transfer of data blocks having intervals across a clock boundary between a first clock domain and a second clock domain (Abstract, 1st 4 lines; column 1, lines 6 – 9; Fig. 1, element 14 clock rate CLK Y and element 12 at clock rate CLK X), wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal (Figs. 1 & 2, CLK y and CLK X) , said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M>1 (Fig. 4, CLK Y comprising 9 clock cycles to CLK X comprising 8 clock cycles; wherein N = 9 and M = 8) , comprising:

a first circuit portion for providing said data blocks to a second circuit portion (Fig. 2, elements 14 and 12; column 2, lines 49 – 54; wherein the first circuit is element 14 and the second circuit is element 12) ;

a synchronizer controller disposed between said first and second clock domains for providing at least one dead cycle control signal to said second circuit portion, wherein said at least one dead cycle control signal is indicative of the location of at least one dead cycle between said first and second clock signal (Fig. 2, element 16; Fig. 3; Fig. 4, element HIGH STROBE; wherein the synchronizer controller is interpreted as the

detection module 16 which generates the LOW STROBE and HIGH STROBE outputs and the HIGH STROBE output indicates the position of the dead cycle, as shown in Fig. 4);

whereby said data blocks are transmitted as contiguous data blocks relative to said at least one dead cycle (Fig. 4, data blocks transmitted according to HIGH STROBE).

Garcia doesn't disclose control logic for generating data transfer control signals.

In the same field of endeavor, however, Audityan discloses control logic associated with said second circuit portion for generating data transfer control signals responsive to said at least one dead cycle control signal, said data transfer control signals for controlling said second circuit portion (Fig. 1, element 51 output that controls the mux 19 which receives data from the queue 16; column 5, lines 25 – 39, 52 – 60; column 7, lines 17 – 27; wherein the control logic is interpreted as the decoder 19, the data control signals are interpreted as the output of the decoder that control the selection from the queue 16 and the input to the decoder 51 is interpreted as the dead cycle control signal).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Audityan, in the system of Garcia because this would allow the appropriate data element from the queue to be selected, as disclosed by Audityan (same column, line numbers as above).

Regarding claim 3, Garcia does not disclose a mux and a queue of data blocks.

In the same field of endeavor, however, Audityan discloses said second circuit portion comprises:

at least one queue operably coupled to said first circuit portion for temporarily storing said data blocks (Fig. 1, element 16, 17 which receives the data; column 5, lines 25 – 39, 52 – 60; column 7, lines 17 – 27) ;

and a multiplexer (MUX) block operably coupled to said first circuit portion and said at least one queue, said MUX block operating under a MUX selection control signal generated by said control logic for selecting between data blocks stored in said at least one queue and data blocks provided by said first circuit portion without queuing, whereby said data blocks are transmitted as an output of said MUX block to a synchronizer operating under control of said synchronizer controller (Fig. 1, elements 19, 51; column 5, lines 25 – 39, 52 – 60; column 7, lines 17 – 27; wherein the mux is element 19 that selects one of the queue entries).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Audityan, in the system of Garcia because this would allow the appropriate data element from the queue to be selected, as disclosed by Audityan (same column, line numbers as above).

Regarding claim 5, Garcia discloses each of said data blocks comprises multiple bits (column 4, lines 25 - 29).

Regarding claim 9, Garcia discloses at least one dead cycle comprises N-M dead cycles (Fig. 4, CLK Y and CLK X waveforms; where CLK Y has 9 clock cycles and CLK X has 8 clock cycles, giving 1 dead cycle).

Regarding claim 10, Garcia discloses at least one of said data blocks is positioned adjacent to said at least one dead cycle (Fig. 4, HIGH STROBE signal shows data positioned near DEAD CYCLE).

Regarding claim 11, Garcia discloses the dead cycle control signal is provided 0 to N-1 cycles prior to said dead cycle (Fig. 4, HIGH STROBE signal which shows location of dead signal 0 cycles before dead cycle).

Claim 12 is similarly analyzed as corresponding limitations in claims 1 and 10.

Claim 16 is similarly analyzed as claim 1.

Claims 13, 14, 15 and 17 limitations are similarly analyzed as the corresponding limitations in claim 3.

Claim 18 is similarly analyzed as claim 17, with core clock domain being and bus clock domains being interpreted as the 1st and 2nd clock domains.

Claim 19 is directed to method/steps of the same subject matter claimed in apparatus claim 1 and therefore, is rejected as explained in the rejection of claim 1 above.

Claims 20 - 22 are directed to method/steps of the same subject matter claimed in apparatus claims 9, 11 and 10 respectively and therefore, are rejected as explained in the rejections of claims 9, 11 and 10 above.

Claim 23 is similarly analyzed as claim 19.

4. Claims 2, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Garcia et al. (US 6,084,934)** in view of **Audityan et al. (US 6,317,806)** and further in view of **Warren (US 6,249,875).**

Regarding claim 2, Garcia does not disclose a packet interface.

In the same field of endeavor, however, Warren discloses said first circuit portion comprises a packet interface (Fig. 1, element 14; column 4, lines 39 – 48, 53 – 57; wherein the packet interface is interpreted as the first buffer 14).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Warren, in the system of Garcia because this would allow the input data to be received and stored in a buffer, as disclosed by Warren.

Regarding claim 4, Garcia does not disclose that the data block comprises 1 bit.

In the same field of endeavor, however, Warren discloses each of said data blocks comprises one bit (column 1, lines 20 -28; column 2, lines 3 - 10).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Warren, in the system of Garcia because this would allow processing of a bit stream input , as disclosed by Warren.

5. Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Garcia et al. (US 6,084,934)** in view of **Audityan et al. (US 6,317,806)** and further in view of **Velasco et al. (US 6,115,823).**

Regarding claim 6, Garcia does not disclose that the data block comprises a header that provides protocol control information.

In the same field of endeavor, however, Velasco discloses said data blocks comprise a header that provides protocol control information relative to said data blocks (column 21, lines 58 - 61).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Velasco, in the system of Garcia because this would allow for protocol information to be passed in the header, as is well known in the art.

6. Claims 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Garcia et al. (US 6,084,934)** in view of **Audityan et al. (US 6,317,806)** and further in view of **Velasco et al. (US 6,115,823)** and **Jordan (US 20030016697).**

Regarding claim 7, Garcia does not disclose that the header is removed.

In the same field of endeavor, however, Jordan discloses said header is removed from said header blocks for processing by said control logic (paragraph 83, lines 4 - 5).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Jordan, in the system of

Garcia because the header contains protocol information and it does not need to be processed further once decoded, as is well known in the art.

Allowable Subject Matter

7. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf DSouza whose telephone number is 571-272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER